element array,

wherein said horizontal scanning circuit and said vertical scanning circuit comprise poly-crystal thin-film transistors, and said picture element array, said horizontal scanning circuit and said vertical scanning circuit are formed on a same insulating substrate, and

means for selectively controlling luminance of said picture elements.

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REMARKS

Claims 1 - 18 remain active in this application. The withdrawal of the previous objections and grounds of rejection and the indication of allowability of claims 9 - 14 and 17 are noted with appreciation. Claim 15 has been amended to include subject matter of some recitations of claim 1 as originally presented and as amended previously. No new matter has been introduced into the application.

Claims 1 - 3 have been rejected under 35 U.S.C §103 as being unpatentable over Ito et al. in view of Kuribayashi et al.; claims 4 - 8 have been rejected under 35 U.S.C. §103 as being unpatentable over Ito et al. and Kuribayadhi et al. in view of Fork et al.; and claims 15, 16 and 18 have been rejected under 35 U.S.C. 103 as being unpatentable over Ito et al. in view of Fork et al. These grounds of rejection are respectfully traversed since it is respectfully submitted that the newly cited and applied references are only marginally, if at all, more relevant than the admitted prior art and, moreover, do not provide evidence of a level of ordinary skill in the art which would support a conclusion of obviousness of the claimed subject matter considered as a whole.

The invention, as claimed, is directed to a *combination* of features which simultaneously provides a number of meritorious effects. Specifically, the

invention provides an array of light-emitting elements which extends and is selectively controlled in two orthogonal directions by horizontal and vertical scanning circuits including poly-crystal thin film transistors and which are formed on the same insulating substrate, as recited in independent claims 1 and 15. As additionally recited in claim 2, the light-emitting elements are organic electroluminescent devices which can be manufactured at increased yield (and thus relatively reduced cost) as compared with semiconductor light-emitting diodes or laser diodes but which have reduced luminosity relative to those types of devices when driven in a manner consistent with acceptable useable lifetimes. The extension of the light emitting array in two orthogonal directions allows compensation for low luminosity as well as production of gray scale and continuous tone color printing. The inclusion of both horizontal and vertical scanning circuits on the same substrate provides manufacturing economy and facilitates miniaturization, particularly by reducing the number of required connections to the print head when a matrix array of light-emitting elements is employed, and, in turn, avoids the necessity of fine adjustment by avoiding a need for head replacement through extending lifetime of the light emitter array by operation at low luminosity even though a matrix array of comparatively greater size (and with more connections to a greater number of light-emitting devices in the absence of formation of horizontal and vertical scanning circuits on the same substrate) would be required in order to do so.

For a full appreciation of the merits of the invention derived from the recited combination of features, it should be understood that, prior to the present invention, thin-film poly-crystal transistors were not used for scanning circuits where switching speed and other electrical properties are much more

critical than in the array itself for switching individual light-emitting elements. At the same time, poly-crystal thin film transistors were substantially the only technology which could be formed on the same insulating substrate with organic electroluminescent devices. Conversely, higher performance transistors of conventional designs could be formed on semiconductor substrates together with semiconductor light-emitting devices such as light-emitting diodes and laser diodes but only at the cost of substantially reduced manufacturing yields due largely to substrate imperfections and technical limitations on chip size and packaging as discussed at pages 3 and 4 of the present application. (It should be recalled that arrays must contain a relatively large number of devices and defects in a very small number of such devices can render an entire chip unacceptable for use; resulting in much reduced manufacturing yield and greatly increased cost as arrays are made larger.) Light-emitting diodes and laser diodes also have only a limited ability to produce gray scale and continuous tone printing and also have limited useable lifetimes.

Knowledge of these trade-offs between transistor technologies, manufacturing yield, useable lifetime and maintenance costs and capability, manufacturing and packaging costs, miniaturization, and performance for gray scale and continuous tone printing, as disclosed in the "Background" section of the present application, represent the limit of the state of the art prior to the present invention. This limit on the state of the art is entirely consistent with that evidenced by the references now applied against the claims by the Examiner and it is respectfully submitted that no solution to these trade-offs is provided by the prior art of record. Therefore, it is respectfully submitted that the level of ordinary skill in the art as evidenced by the prior art applied against the claims

by the Examiner does not support a conclusion of obviousness of the *combination of features* claimed.

Specifically, Ito et al. teaches an array of *semiconductor* light-emitting devices such as light-emitting diodes and laser diodes and includes scanning circuits formed of transistors of conventional semiconductor device technologies (but not poly-crystal thin-film transistors) on the same *semiconductor* substrate. Kuribayashi et al. and Fork et al. teach organic electroluminescent devices and Kuribayashi et al. teaches inclusion of poly-crystal thin film transistors in the light-emitting device array but not in horizontal and/or vertical scanning circuits or any other peripheral circuit formed on the same insulating substrate. In particular, it is believed significant that in column 11, lines 51 - 62, of Kuribayashi et al., it is indicated that bias control lines are preferably provided on the insulating substrate and connected to gate array 121 without *any* mention of

1.) any scanning function for the gate array 121,

2.)the technology of the transistors of the gate array,

3.) the physical location of the gate array,

4.) suitability of thin film poly-crystal transistors for use in the gate array, or

5.) any meritorious function or advantage to be derived from any particular choice for any gate array function, transistor technology or gate array physical location, whatsoever.

Thus it is clear that the combination of Ito et al. with Kuribayashi et al. and/or Fork et al. does not, in fact, answer the claimed *combination of features* distinguishing the invention and, moreover, the level of ordinary skill in the art evidenced thereby does not extend to use of poly-crystal thin film transistors in scanning circuits formed on the same insulating substrate with the light-emitting array

and therefore does not support a conclusion of obviousness of inclusion of those features in combination, as recited in the claims. Accordingly, the Examiner's application of the newly cited prior art is clearly seen to be grounded in impermissible hindsight. By the same token, the Examiner has failed to make showing of motivation for the combination of references applied or a *prima facie* demonstration of obviousness of any claim in the application by showing any teaching or suggestion in the references which would lead to an expectation of success in achieving all (or any) of the meritorious effects of the invention which are fully supported by the claimed subject matter.

In other words, the Examiner has found the combination of peripheral circuits formed using *conventional semiconductor transistor technology* on a semiconductor substrate with a *semiconductor* light-emitting (e.g. LEDs or laser diodes) array in one reference and a combination of organic electroluminescent devices with thin film poly-crystal devices *in the array* in another reference and *extrapolated* the extension of the use of thin film poly-crystal of the latter to the peripheral/scanning circuits of the former by *assuming* the suitability of thin-film poly-crystal transistors for scanning circuits to be known and the advantages to be derived from their formation on the same insulating substrate with the light-emitting device array to be recognized within the level of ordinary skill evidenced by the references relied upon when, in fact, those teachings are to be found only in the present application. To the contrary, as pointed out above, omission of such teachings in Kuribayashi et al., particularly at column 11, lines 51 - 62, is a very strong indication that the level of ordinary skill in the art did <u>not</u> extend sufficiently to support the conclusion of

obviousness that the Examiner has stated. Therefore, it is respectfully submitted that the rejections of record are improper and in error and, upon reconsideration, withdrawal thereof is respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,

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APPENDIX

15. (Amended) An optical printer head comprising:

a picture element array comprising picture elements containing light emitting devices arranged in directions of a picture element line and a picture element string in two dimensions;

a horizontal scanning circuit to feed data signals to each picture element string in said picture element array;

a vertical scanning circuit to sequentially select and activate each picture element line in said picture element array,

wherein said horizontal scanning circuit and said vertical scanning circuit comprise poly-crystal thin-film transistors, and said picture element array, said horizontal scanning circuit and said vertical scanning circuit are formed on a same insulating substrate, and

means for selectively controlling luminance of said picture elements.